Digital System Design Lab Subject Code: NECC104

Sl No.	Name of the Experiments	No of Week
01	Design and hardware implementation of Half Adder and Full Adder using NAND gates.	01
02	Design and hardware implementation of Half Subtractor and Full Subtractor Using NAND gates.	02
03	Design and hardware implementation of 4:1 Multiplexer using universal gates and realization of Full Adder using Multiplexers.	01
04	Design and hardware implementation of BCD Adder using two binary adders (IC based) and other gates.	01
05	Design and hardware implementation of 3:8 Decoder and realization of Full Adder.	01
06	Realization of R-S, D ,J-K and T latches and Flip-Flops	01
07	Realization of J-K (Master-Slave) Flip Flop	01
08	Realization of Mod-8 Up-Down Ripple Counter.	01
09	Realization of synchronous Mod-3 and Mod-2 counters	01
10	Realization of higher Mod counter by cascading lower Mod counters.	01
11	Mini project based on Digital Electronics Component.	02
12	End Semester Lab Examination and Viva – Voce	01